M61323SP/FP

Wide Frequency Band Analog Switch

REJ03F0201-0201
Rev.2.01
Mar 31, 2008

Description

The M61323SP/FP is a semiconductor integrated circuit for the RGBHV interface. The device features switching signals input from two types of image sources and outputting the signals to the CRT display, etc. Synchronous signals, meeting a frequency band of 10 kHz to 200 kHz, are output at TTL. The frequency band of video signals is 250 MHz, acquiring high-resolution images, and are optimum as an interface IC with high-resolution CRT display and various new media.

The M61323SP/FP keeps the power saving mode, and it can reduce I_{CC} about 10 mA under the condition that all V_{CC} are supplied.

Features

- Frequency band : RGB 250 MHz
  H, V 10 kHz to 200 kHz
- Input level: RGB 0.7 V_{P-P} (Typ.)
  H, V TTL input 3 to 5 V_{O-P} (bipolar)
- Only the G channel is provided with Sync-on video output. The TTL format is adopted for HV output.

Application

Display monitor

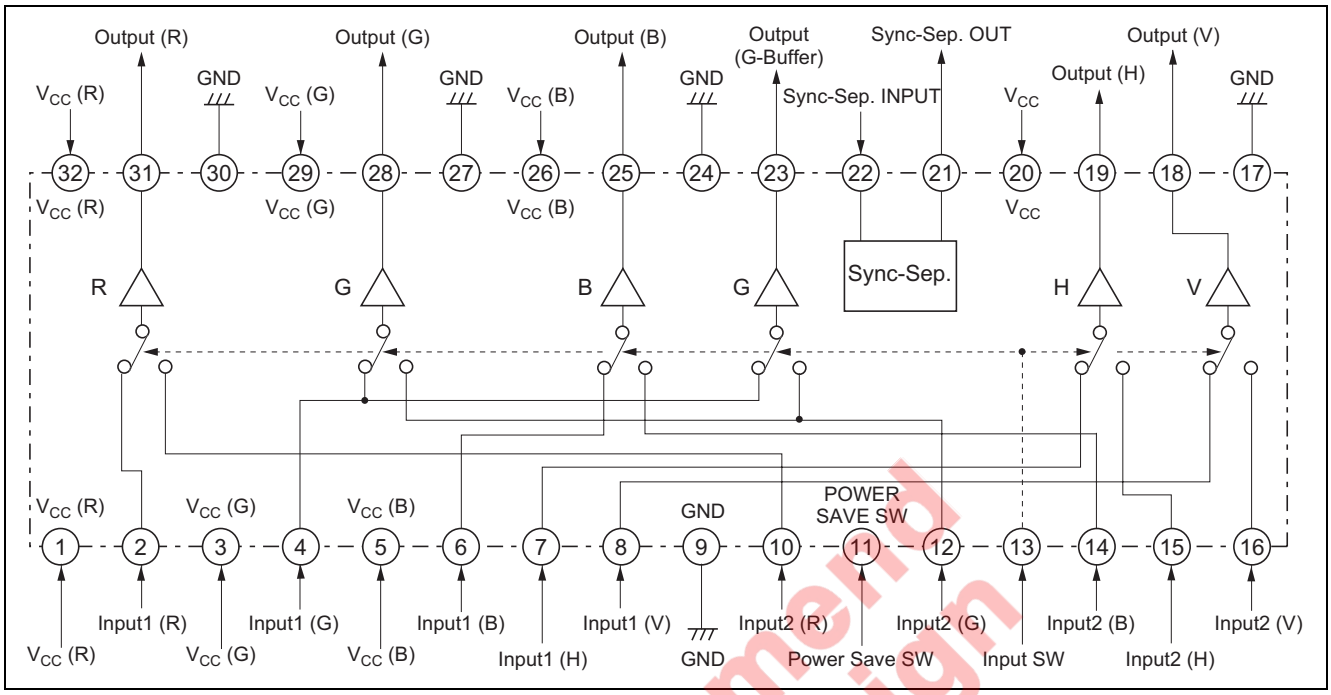
Recommended Operating Condition

Supply voltage range: 4.75 to 5.25 V

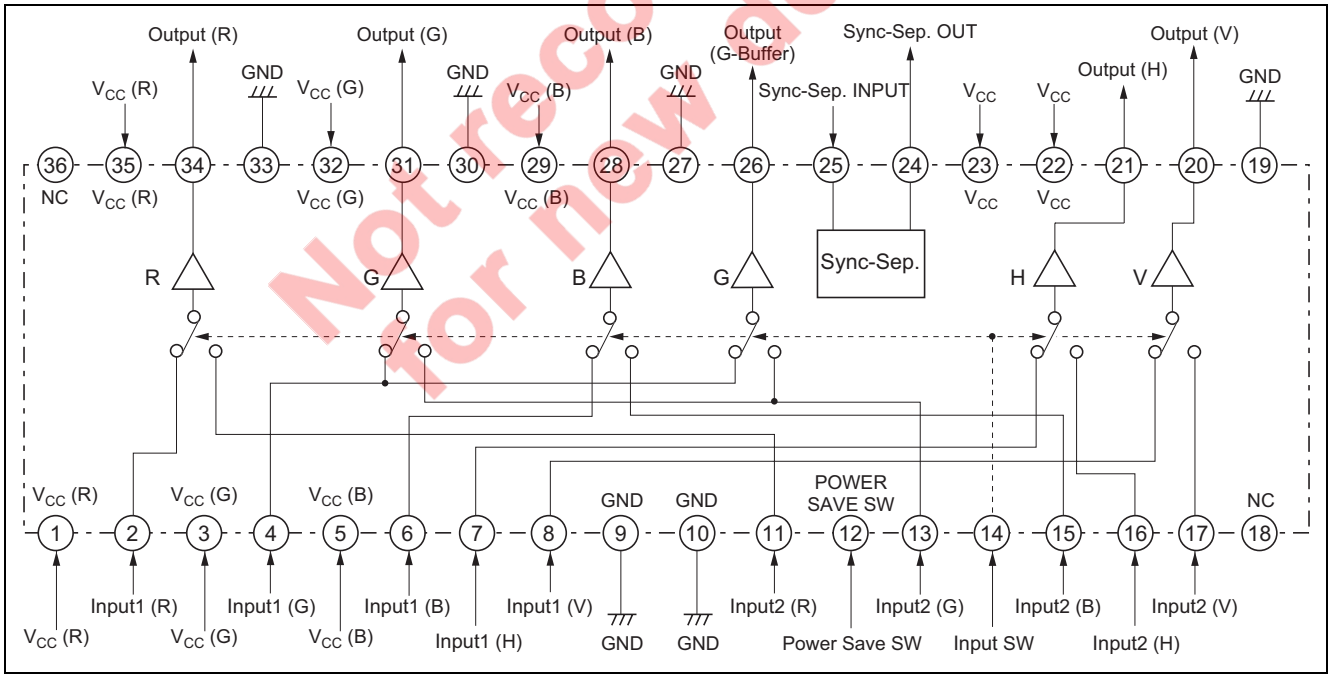
Rated voltage range: 5.0 V

Block Diagram

M61323SP

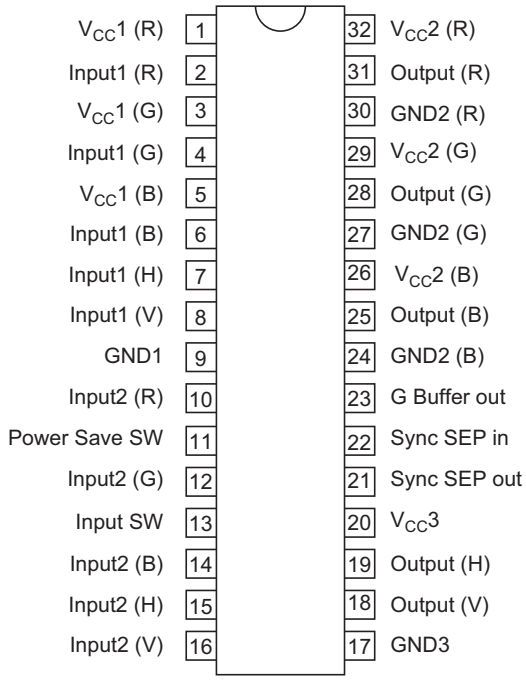


M61323FP



Pin Arrangement

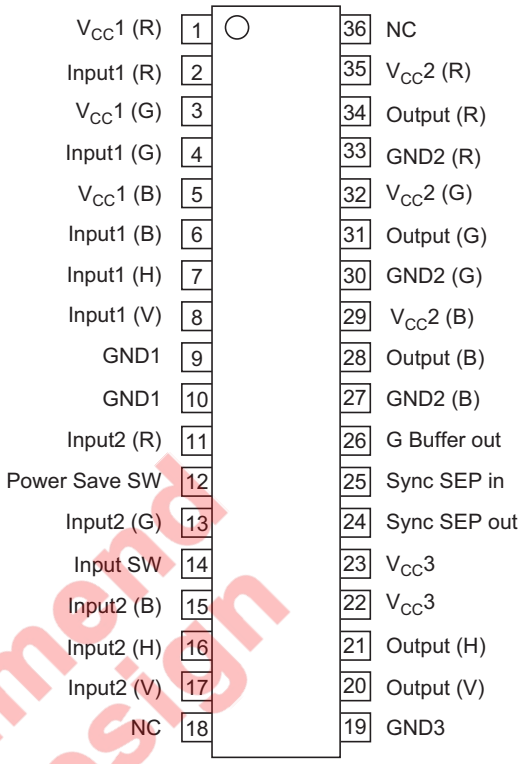
M61323SP



(Top view)

Outline: PRDP0032BA-A (32P4B)

M61323FP



(Top view)

Outline: PRSP0036GA-B (36P2R-D)

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7.0	V
Power dissipation	Pd	1603 (SP), 1068 (FP)	mW
Operating temperature	Topr	–20 to +85 (SP), –20 to +75 (FP)	°C
Storage temperature	Tstg	–40 to +150	°C
Electrostatic discharge	Surge	±200	V
Recommended supply voltage	Vopr	5.0	V
Recommended supply voltage range	Vopr'	4.75 to 5.25	V

Electrical Characteristics

(M61323SP V_{CC} = 5.0 V, Ta = 25°C)

Item	Symbol	Limits			Unit	Test Point (s)	Input											SW	
		Min.	Typ.	Max.			SW2 Rin1	SW4 Gin1	SW6 Bin1	SW7 Hin1	SW8 Vin1	SW10 Rin2	SW12 Gin2	SW14 Bin2	SW15 Hin2	SW16 Vin2	SW22 Sync	SW11 P.sav	SW13 Switch
Circuit current1	I_{CC}	—	70	—	mA	—	b	b	b	b	b	b	b	b	b	b	b	a 3 V	b
Circuit current2	I_{CC}STBY	—	—	10	mA	—	b	b	b	b	b	b	b	b	b	b	b	b	b
RGB SW																			
Output DC voltage1	Vdc1	—	1.5	—	V	31 28 25	b	b	b	b	b	b	b	b	b	b	b	a 3 V	b
Output DC voltage2	Vdc2	—	1.5	—	V	31 28 25	b	b	b	b	b	b	b	b	b	b	b	a 3 V	a 3 V
Output DC voltage3	Vdc3	—	0.9	—	V	23	b	b	b	b	b	b	b	b	b	b	b	a 3 V	b
Output DC voltage4	Vdc4	—	0.9	—	V	23	b	b	b	b	b	b	b	b	b	b	b	a 3 V	a 3 V
Maximum allowable input level1	Vimax1	—	1.8	—	V_{P-P}	31 28 25	abb SG1	bab SG1	bba SG1	b	b	b	b	b	b	b	b	a 3 V	b
Maximum allowable input level2	Vimax2	—	1.8	—	V_{P-P}	31 28 25	b	b	b	b	b	abb SG1	bab SG1	bba SG1	b	b	b	a 3 V	a 3 V
Voltage gain1	G_{V1}	–0.1	0.7	1.3	dB	31 28 25	abb SG2	bab SG2	bba SG2	b	b	b	b	b	b	b	b	a 3 V	b
Relative voltage gain1	ΔG_{V1}	–0.4	0	0.4	dB	—	Relative to measured values above												
Voltage gain2	G_{V2}	–0.1	0.7	1.3	dB	31 28 25	b	b	b	b	b	abb SG2	bab SG2	bba SG2	b	b	b	a 3 V	a 3 V
Relative voltage gain2	ΔG_{V2}	–0.4	0	0.4	dB	—	Relative to measured values above												
Voltage gain3	G_{V3}	–0.6	0	0.6	dB	23	b	a SG2	b	b	b	b	b	b	b	b	b	a 3 V	b
Voltage gain4	G_{V4}	–0.6	0	0.6	dB	23	b	b	b	b	b	b	a SG2	b	b	b	b	a 3 V	a 3 V

Electrical Characteristics (cont.)

Item	Symbol	Limits			Unit	Test Point (s)	Input											SW	
		Min.	Typ.	Max.			SW2 Rin1	SW4 Gin1	SW6 Bin1	SW7 Hin1	SW8 Vin1	SW10 Rin2	SW12 Gin2	SW14 Bin2	SW15 Hin2	SW16 Vin2	SW22 Sync	SW11 P.sav	SW13 Switch
Freq. characteristic1 (100 MHz)	F_{C1}	–1	0	1	dB	31 28 25	abb SG4	bab SG4	bba SG4	b	b	b	b	b	b	b	b	a 3 V	b
Relative Freq.characteristic1 (100 MHz)	ΔF_{C1}	–1	0	1	dB	—	Relative to measured values above												
Freq.characteristic2 (100 MHz)	F_{C2}	–1	0	1	dB	31 28 25	b	b	b	b	b	abb SG4	bab SG4	bba SG4	b	b	b	a 3 V	a 3 V
Relative Freq.characteristic2 (100 MHz)	ΔF_{C2}	–1	0	1	dB	—	Relative to measured values above												
Freq.characteristic3 (250 MHz)	F_{C3}	–3	—	—	dB	31 28 25	abb SG5	bab SG5	bba SG5	b	b	b	b	b	b	b	b	a 3 V	b
Freq.characteristic4 (250 MHz)	F_{C4}	–3	—	—	dB	31 28 25	b	b	b	b	b	abb SG5	bab SG5	bba SG5	b	b	b	a 3 V	a 3 V
Crosstalk between two inputs1 (10 MHz)	C.T.I.1	—	–60	–45	dB	31 28 25	abb SG3	bab SG3	bba SG3	b	b	b	b	b	b	b	b	a 3 V	a 3 V
Crosstalk between two inputs2 (10 MHz)	C.T.I.2	—	–60	–45	dB	31 28 25	b	b	b	b	b	abb SG3	bab SG3	bba SG3	b	b	b	a 3 V	b
Crosstalk between two inputs3 (100 MHz)	C.T.I.3	—	–40	–30	dB	31 28 25	abb SG4	bab SG4	bba SG4	b	b	b	b	b	b	b	b	a 3 V	a 3 V
Crosstalk between two inputs4 (100 MHz)	C.T.I.4	—	–40	–30	dB	31 28 25	b	b	b	b	b	abb SG4	bab SG4	bba SG4	b	b	b	a 3 V	b
Crosstalk between channels1 (10 MHz)	C.T.C1	—	–50	–40	dB	31 28 25	abb SG3	bab SG3	bba SG3	b	b	b	b	b	b	b	b	a 3 V	b
Crosstalk between channels2 (10 MHz)	C.T.C2	—	–50	–40	dB	31 28 25	b	b	b	b	b	abb SG3	bab SG3	bba SG3	b	b	b	a 3 V	a 3 V
Crosstalk between channels3 (100 MHz)	C.T.C3	—	–30	–25	dB	31 28 25	abb SG4	bab SG4	bba SG4	b	b	b	b	b	b	b	b	a 3 V	b
Crosstalk between channels4 (100 MHz)	C.T.C4	—	–30	–25	dB	31 28 25	b	b	b	b	b	abb SG4	bab SG4	bba SG4	b	b	b	a 3 V	a 3 V
Pulse characteristic1	Tr1	—	1.6	2.5	ns	31 28 25	abb SG6	bab SG6	bba SG6	b	b	b	b	b	b	b	b	a 3 V	b
	Tf1	—	1.6	2.5	ns	31 28 25	abb SG6	bab SG6	bba SG6	b	b	b	b	b	b	b	b	a 3 V	b
Pulse characteristic2	Tr2	—	1.6	2.5	ns	31 28 25	b	b	b	b	b	abb SG6	bab SG6	bba SG6	b	b	b	a 3 V	a 3 V
	Tf2	—	1.6	2.5	ns	31 28 25	b	b	b	b	b	abb SG6	bab SG6	bba SG6	b	b	b	a 3 V	a 3 V

Electrical Characteristics (cont.)

Item	Symbol	Limits			Unit	Test Point (s)	Input											SW	
		Min.	Typ.	Max.			SW2 Rin1	SW4 Gin1	SW6 Bin1	SW7 Hin1	SW8 Vin1	SW10 Rin2	SW12 Gin2	SW14 Bin2	SW15 Hin2	SW16 Vin2	SW22 Sync	SW11 P.sav	SW13 Switch
HV SW																			
High level output voltage1	Vdch1	3.8	4.2	—	V	18 19	b	b	b	a SG8	a SG8	b	b	b	b	b	b	a 3 V	b
High level output voltage2	Vdch2	3.8	4.2	—	V	18 19	b	b	b	b	b	b	b	b	a SG8	a SG8	b	a 3 V	a 3 V
Low level output voltage1	Vdcl1	—	0.2	0.5	V	18 19	b	b	b	a SG8	a SG8	b	b	b	b	b	b	a 3 V	b
Low level output voltage2	Vdcl2	—	0.2	0.5	V	18 19	b	b	b	b	b	b	b	b	a SG8	a SG8	b	a 3 V	a 3 V
Input threshold voltage H	VithH	1.8	2.0	2.2	V	18 19	b	b	b	a SG8	a SG8	b	b	b	b	b	b	a 3 V	b
Input threshold voltage L	VithL	1.0	1.4	1.6	V	18 19	b	b	b	a SG8	a SG8	b	b	b	b	b	b	a 3 V	b
Rising time3	Tr3	—	25	—	ns	18 19	b	b	b	a SG8	a SG8	b	b	b	b	b	b	a 3 V	b
Falling time3	Tf3	—	15	—	ns	18 19	b	b	b	a SG8	a SG8	b	b	b	b	b	b	a 3 V	b
Rising delay time	HVDr	—	40	60	ns	18 19	b	b	b	a SG8	a SG8	b	b	b	b	b	b	a 3 V	b
Falling delay time	HVDf	—	40	60	ns	18 19	b	b	b	a SG8	a SG8	b	b	b	b	b	b	a 3 V	b
Sync SEP.																			
Sync on G input minimum voltage	SYrv	0.2	—	—	V_{P-P}	21	b	b	b	b	b	b	b	b	b	b	a SG7	a 3 V	—
Sync output high level voltage	SYVH	3.8	4.3	—	V	21	b	b	b	b	b	b	b	b	b	b	a SG7	a 3 V	—
Sync output low level voltage	SYVL	—	0.2	0.5	V	21	b	b	b	b	b	b	b	b	b	b	a SG7	a 3 V	—
Sync output rising time 3	STr	—	25	—	ns	21	b	b	b	b	b	b	b	b	b	b	a SG7	a 3 V	—
Sync output falling time 3	STf	—	15	—	ns	21	b	b	b	b	b	b	b	b	b	b	a SG7	a 3 V	—
Sync output rising delay time	SDr	—	40	60	ns	21	b	b	b	b	b	b	b	b	b	b	a SG7	a 3 V	—
Sync output falling delay time	SDf	—	40	60	ns	21	b	b	b	b	b	b	b	b	b	b	a SG7	a 3 V	—
Channel Select SW, Power Save SW																			
Channel select SW threshold voltage1	Vthch1	2.5	—	—	V	—	a SG6	a SG6	a SG6	a SG8	a SG8	b	b	b	b	b	a SG7	a 3 V	a variable
Channel select SW threshold voltage2	Vthch2	—	—	1.0	V	—	a SG6	a SG6	a SG6	a SG8	a SG8	b	b	b	b	b	a SG7	a 3 V	a variable
Power save SW threshold voltage1	VthPH	2.0	—	—	V	—	a SG6	a SG6	a SG6	a SG8	a SG8	b	b	b	b	b	a SG7	a variable	b
Power save SW threshold voltage2	VthPL	—	—	1.0	V	—	a SG6	a SG6	a SG6	a SG8	a SG8	b	b	b	b	b	a SG7	a variable	b

Electrical Characteristics Test Method (M61323SP)

Circuit Current 1

No signal. Measure the total circuit current as I_{CC} when supplying 3 VDC to pin 11.

Circuit Current 2

No signal. Measure the total circuit current as I_{CC}STBY when pin 11 connected to GND.

Output DC Voltage 1, 2

Set SW13 to GND (or OPEN), measure the DC voltage of TP31 (TP28, TP25) when there is no signal input.

The DC voltage is as vdc1 (vdc2).

Output DC Voltage 3, 4

Measure the DC voltage TP23 same as "Output DC voltage 1, 2". The DC voltage is Vdc3 (Vdc4).

Maximum Allowable Input Level 1, 2

Set SW13 to GND, input SG1 to pin 2 only. Gradually increasing the SG1 amplitude, read the amplitude of the input signal when the output waveform of TP31 is strained. The value is as Vimax1. In the same way, measure Vimax1 in response to inputs in pin 4 and pin 6 only.

Then set SW13 to OPEN, measure Vimax2 in response to inputs in pin 10, 12 and 14 only.

Voltage Gain 1, 2

1. The conditions is as table.
2. Set SW13 to GND, input SG2 (0.7 V_{P-P}) to pin 2 only. Read the output amplitude of TP31. The value is as $V_{OR}1$.
3. Voltage gain G_{V1} is

$$G_{V1} = 20\log \frac{V_{OR}1\ [V_{P-P}]}{0.7} \quad (dB)$$

4. In the same way, calculate G_{V1} in response to inputs in pin 4 and pin 6 only.
5. Then set SW13 to OPEN, measure G_{V2} in response to inputs in pin l0, 12 and 14 only.

Relative Voltage Gain 1, 2

1. Calculate relative voltage gain ΔG_V1 by the following formula.

$$\Delta G_{V1} = G_{V1}R - G_{V1}G,\ G_{V1}G - G_{V1}B,\ G_{V1}B - G_{V1}R$$

2. In the same way, calculate ΔG_{V2}

Voltage Gain 3, 4

1. The conditions is as table.
2. Read the output amplitude of TP23.
3. Calculate G_{V3}, G_{V4} same as "Voltage gain 1".

Freq. Characteristic 1, 2/Relative Freq. Characteristic 1, 2

1. The conditions is as table. This measurement shall use active probe.
2. Set SW13 to GND, input SG4 (0.7 V_{P-P}) to pin 2 only. Measure TP31 output amplitude as $V_{OR}1$.
   In the same way, input SG2 (0.7 V_{P-P}) to pin 2 only. Measure TP31 output amplitude as $V_{OR}2$.
3. Freq.characteristic1 F_{C1} is

$$F_{C1} = 20\log \frac{V_{OR}2\ [V_{P-P}]}{V_{OR}1\ [V_{P-P}]} \quad (dB)$$

4. In the same way, calculate F_{C1} in response to inputs in pin 4 and pin 6 only.
5. The difference between of each channel Freq.characteristic is as ΔF_{C1}.
6. Then set SW13 to OPEN, measure F_{C2} and ΔF_{C2} in response to inputs in pin 10, 12 and 14 only.

Freq. Characteristic 3, 4

Measure the F_{C3}, F_{C4} when SG5 of input signal. (For reference)

Crosstalk between Two Inputs 1, 2

1. The conditions is as table. This measurement shall use active probe.
2. Set SW13 to GND, input SG3 to pin 2 only. Read the output amplitude of TP31. The value is as $V_{OR}3$.
3. Then set SW13 to OPEN, read the output amplitude of TP31. The value is as $V_{OR}3'$.
4. Crosstalk between two inputs 1 C.T.I.1 is

$$C.T.I.1 = 20\log \frac{V_{OR}3' \, [V_{P-P}]}{V_{OR}3 \, [V_{P-P}]} \quad (dB)$$

5. In the same way, calculate C.T.I.1 in response to inputs in pin 4 and pin 6 only.
6. Then set SW13 to OPEN, input SG2 to pin 10 only. Read the output amplitude of TP31. The value is as $V_{OR}4$.
7. Set SW13 to GND, read the output amplitude of TP31. The value is as $V_{OR}4'$.
8. Crosstalk between two inputs 1 C.T.I.2 is

$$C.T.I.2 = 20\log \frac{V_{OR}4' \, [V_{P-P}]}{V_{OR}4 \, [V_{P-P}]} \quad (dB)$$

9. In the same way, calculate C.T.I.2 in response to inputs in pin 12 and pin 14 only.

Crosstalk between Two Inputs 3, 4

Set SG4 as the input signal, and then the same method as table, measure C.T.I.3, C.T.I.4.

Crosstalk between Channels 1, 2

1. The conditions is as table. This measurement shall use active probe.
2. Set SW13 to GND, input SG3 (0.7 V_{P-P}) to pin 2 only. Read the output amplitude of TP31. The value is as $V_{OR}5$.
3. Next, measure TP28, TP25 in the same state, and the amplitude is as $V_{OG}5$, $V_{OB}5$.
4. Crosstalk between channels1 C.T.C1 is

$$C.T.C1 = 20\log \frac{V_{OG}5 \text{ or } V_{OB}5}{V_{OR}5} \quad (dB)$$

5. In the same way, calculate C.T.C1 in response to inputs in pin 4 and pin 6 only.
6. Then set SW13 to OPEN, input SG3 (0.7 V_{P-P}) to pin 10 only.
   Read the output amplitude of TP31. The value is as $V_{OR}6$.
7. Next, measure TP28, TP25 in the same state, and the amplitude is as $V_{OG}6$, $V_{OB}6$.
8. Crosstalk between two inputs 1 C.T.C2 is

$$C.T.C2 = 20\log \frac{V_{OG}6 \text{ or } V_{OB}6}{V_{OR}6} \quad (dB)$$

9. In the same way, calculate C.T.C2 in response to inputs in pin 9 and pin 11 only.

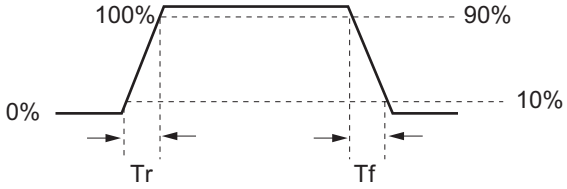
Crosstalk between Channels 3, 4

Set SG4 as the input signal, and then the same method astable, measure C.T.C3, C.T.C4.

Pulse Characteristic 1, 2

1. The conditions is as table (SG5 amplitude 0.7 V_{p-p}). Set SW13 to GND (or OPEN).
2. Measure rising Tri and falling Tfi for 10% to 90% of the input pulse with active probe.
3. Next, measure rising Tro and falling Tfo for 10% to 90% of the output pulse with active probe.
4. Pulse characteristic Tr1, Tf1 (Tr2, Tf2) is

$$Tr1\ (Tr2) = \sqrt{(Tro)^2 - (Tri)^2}\quad (ns)$$
$$Tf1\ (Tf2) = \sqrt{(Tfo)^2 - (Tfi)^2}\quad (ns)$$



<HV-SW>

High Level Output Voltage 1, 2/Low Level Output Voltage 1, 2

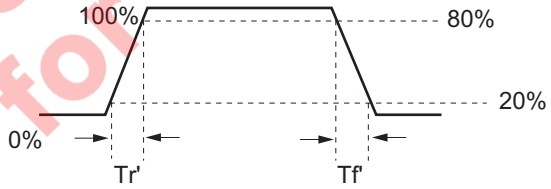
1. The conditions is as table. Input SG8 to pin 7 (or pin 8). Set SW13 to GND, read the output high level and low voltage of TP19, TP18. The value is as Vdch1, Vdcl1.
2. Input SG8 to pin 15 (or pin 16). Set SW13 to OPEN, read the output high level and low voltage of TP19, TP18. The value is as Vdch2, Vdcl2.

Input Threshold Voltage H/Input Threshold Voltage L

1. Set SW13 to GND (or OPEN). Gradually increasing the voltage of pin 7 (or pin 15) from 0 V, measure the input voltage of pin 7 (or pin 15) when the TP19 voltage turned high level (3.8 V or more). The value is as VithH.
2. Gradually decreasing the voltage of pin 7 (or pin 15) from 3 V, measure the input voltage of pin 7 (or pin 15) when the TP19 voltage turned low level (0.5 V or less). The value is as VithL.
3. In the same way, measure the input voltage of pin 8 (or pin 16) as VithH, VithL.

Rising Time/Falling Time

1. The conditions is as table. This measurement shall use active probe.
2. Measure rising Tri and falling Tfi for 20% to 80% of the output pulse as Tr3, Tf3 (Tr4, Tf4).

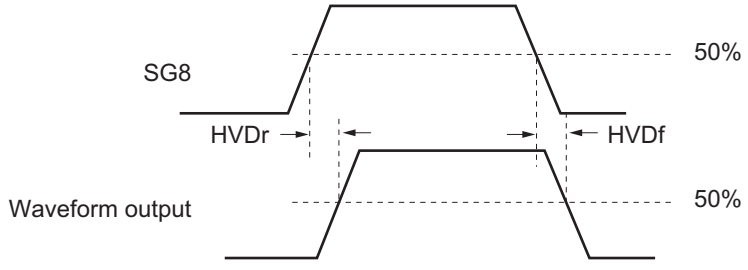


Rising Delay Time/Falling Delay Time

Set SW13 to GND (or OPEN), input SG8 to pin 7 (or pin 15).

Measure the rising delay time HVDr and the falling delay time HVDf.

In the same way, measure HVDr and HVDf when input SG8 to pin 8 (or pin 16)



<Sync-Separation>

Sync Input Minimum Voltage

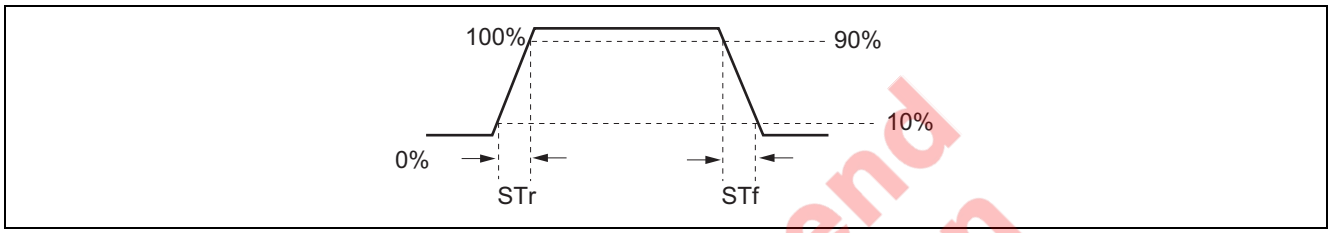
Gradually decreasing the amplitude of SG7 in pin 22, measure the amplitude of SG7 when the Sync-Sep output signal turn off. The value is as SYrv.

Sync Output High Level Voltage/Sync Output Low Level Voltage

Input SG7 to pin 22, read the output high level and low voltage of TP21. The value is as SYVH, SYVL.

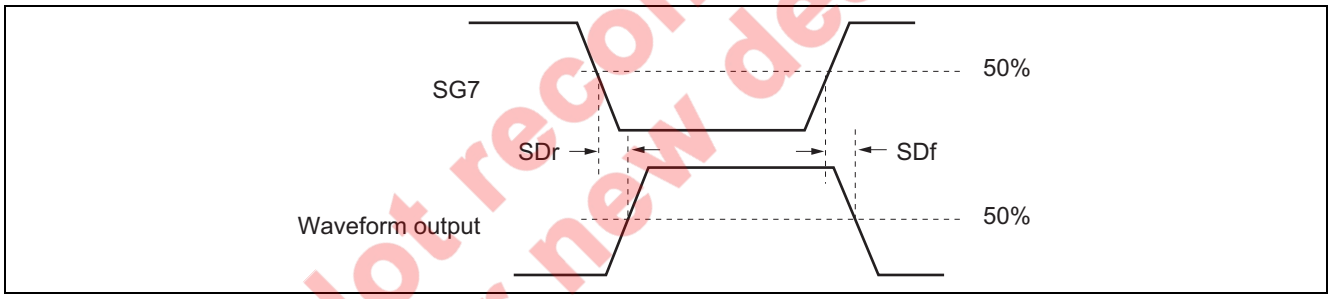
Sync Output Rising Time/Sync Output Falling Time

1. The conditions is as table. (SG7 amplitude 0.3 V_{P-P})
   This measurement shall use active probe.
2. Measure rising Tri and falling Tfi for 10% to 90% of the input pulse as STr, STf.



Sync Output Rising Delay Time/Sync Output Falling Delay Time

Input SG7 to pin 22. Measure the rising delay time SDr and the falling delay time SDf.



<Others>

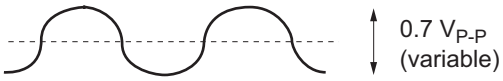
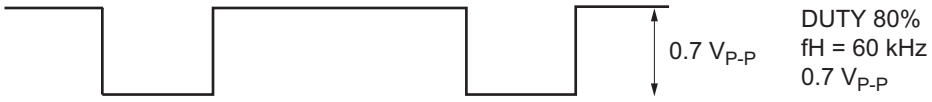
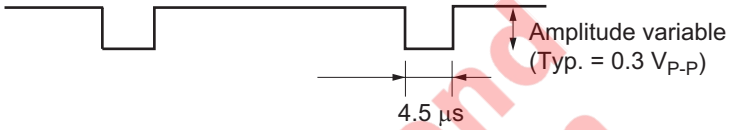
Channel Select SW Threshold 1, 2

1. Gradually increasing the voltage of pin 13 from 0 V, measure the maximum voltage of pin 13 when the channel 1 is selected. The value is as Vthch1.
2. Gradually decreasing the voltage of pin 13 from 5 V, measure the minimum voltage of pin 13 when the channel 2 is selected. The value is as Vthch2.

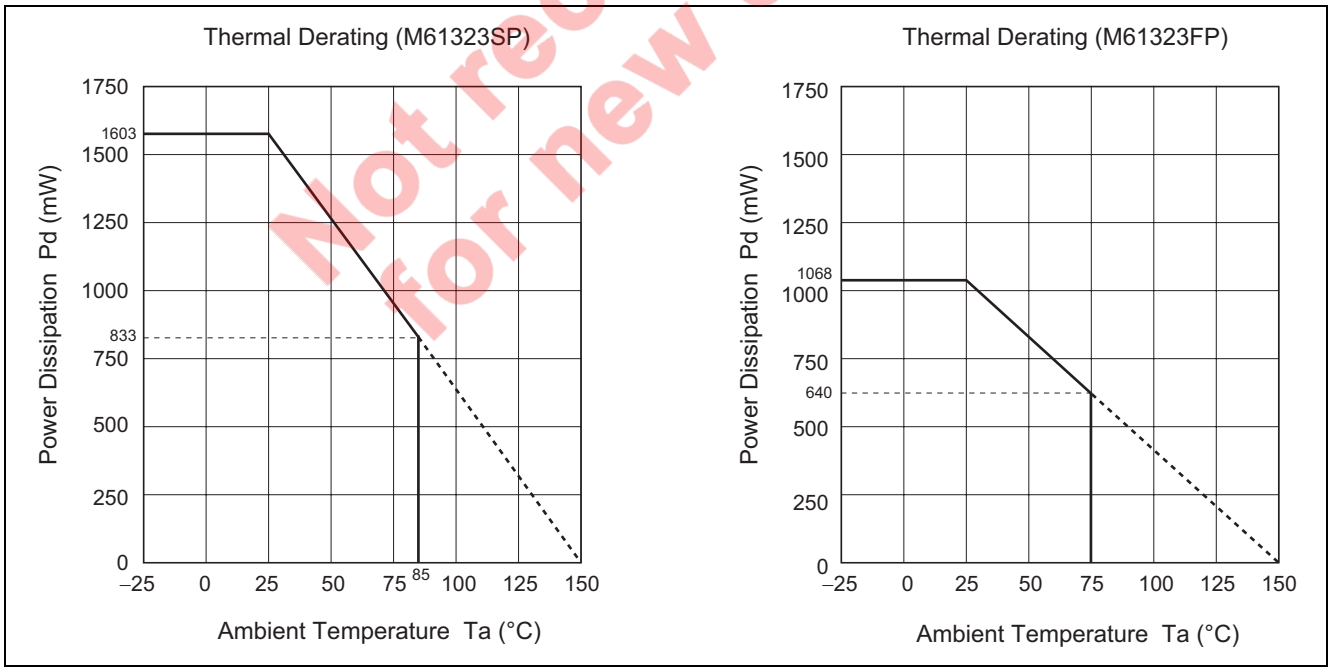
Power Save SW Threshold 1, 2

1. Gradually increasing the voltage of pin 11 from 0 V, measure the maximum voltage of pin 11 when the power save mode. The value is as VthPL.
2. Gradually decreasing the voltage of pin 13 from 5 V, measure the minimum voltage of pin 11 when the power save mode. The value is as VthPH.

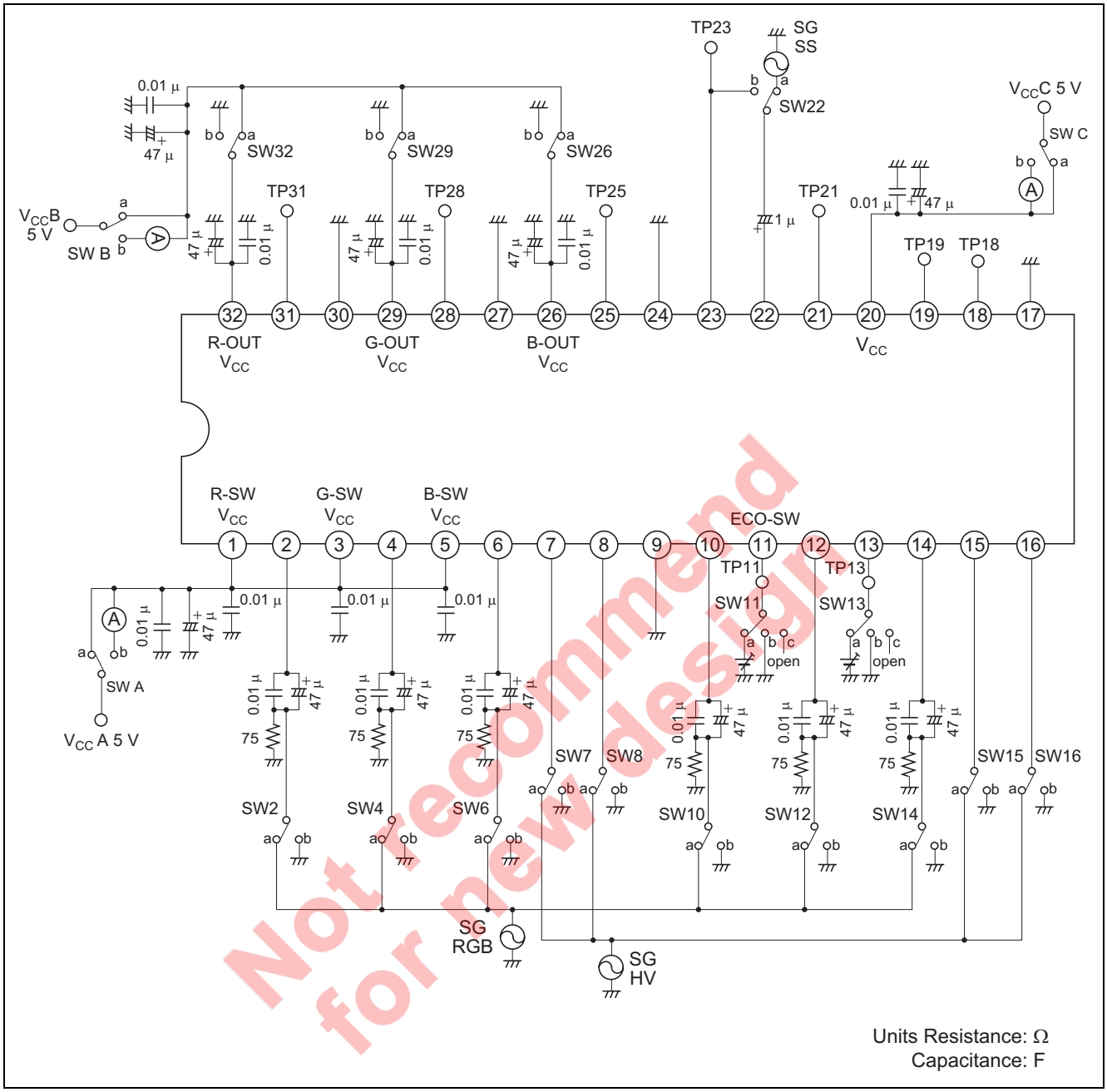
Input Signal

SG No.	Signals
SG1	Sine wave (f = 60 kHz, 0.7 V_{P-P} (Amplitude variable)) 
SG2	Sine wave (f = 1 MHz, 0.7 V_{P-P} (Amplitude variable))
SG3	Sine wave (f = 10 MHz, 0.7 V_{P-P} (Amplitude variable))
SG4	Sine wave (f = 100 MHz, 0.7 V_{P-P} (Amplitude variable))
SG5	Sine wave (f = 250 MHz, 0.7 V_{P-P} (Amplitude variable))
SG6	
SG7	Sync (fH = 60 kHz) 
SG8	

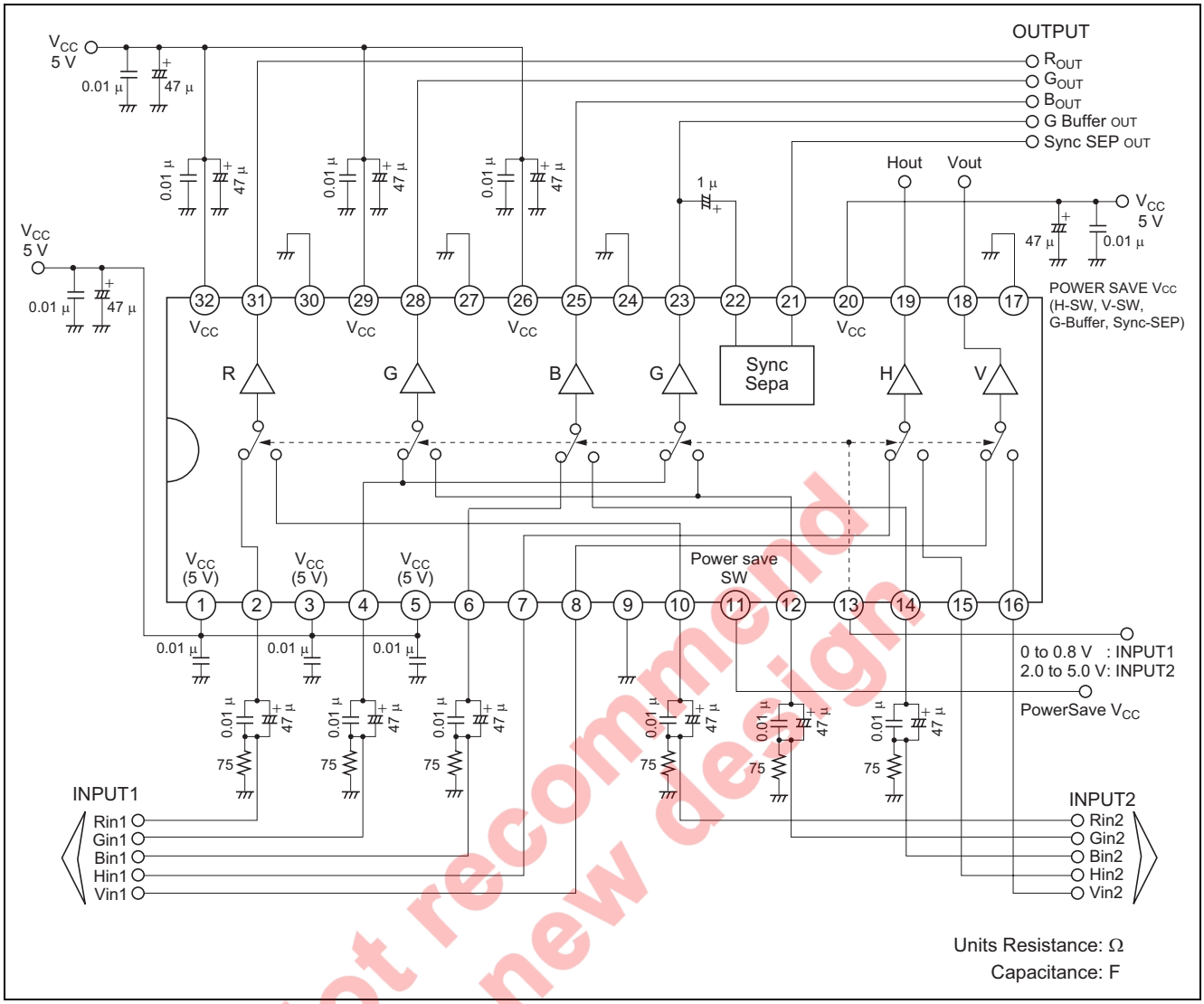
Typical Characteristics



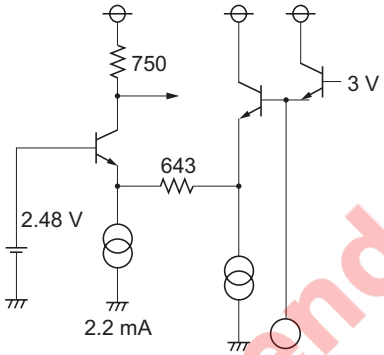
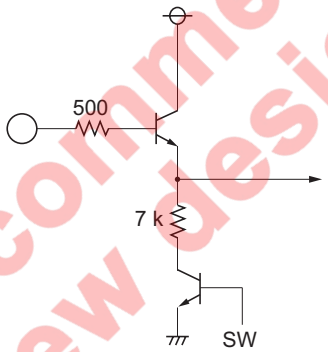
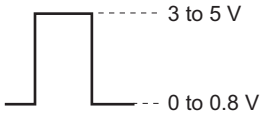
Test Circuit (M61323SP)



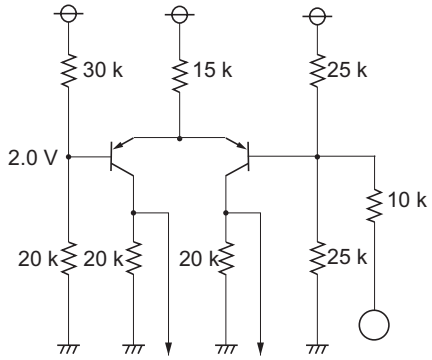
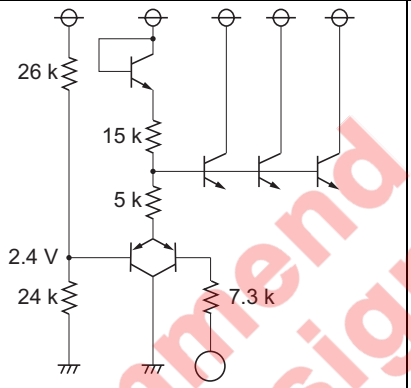
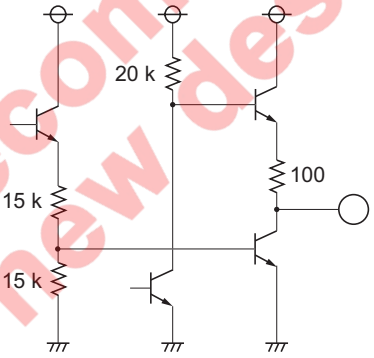
Application Example (M61323SP)



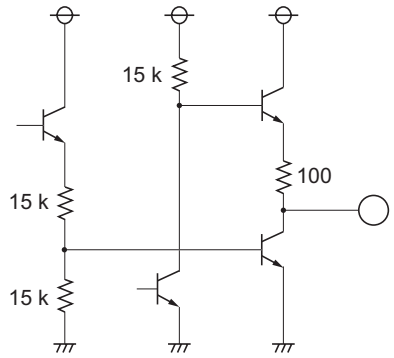
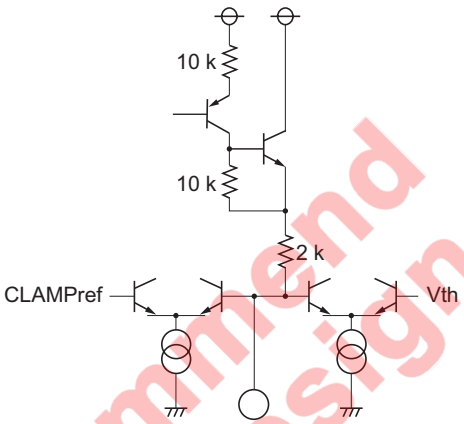
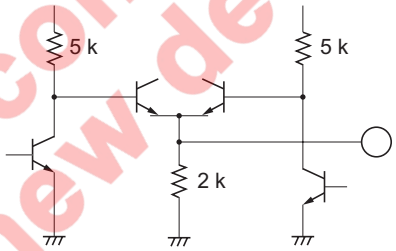
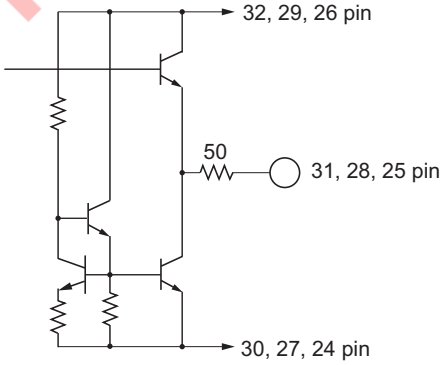
Pin Description (M61323SP)

pin No.	Name	DC Voltage (V)	Peripheral Circuit	Function
1 3 5 20	V_{CC} (R) V_{CC} (G) V_{CC} (B) V_{CC} (H, V, Sync-Sep.)	5.0	—	—
26 29 32	V_{CC} (ROUT) V_{CC} (GOUT) V_{CC} (BOUT)	5.0	—	—
2 4 6 10 12 14	Input1 (R) Input1 (G) Input1 (B) Input2 (R) Input2 (G) Input2 (B)	2.3		Input signal with low impedance
7 8 15 16	Input1 (H) Input1 (V) Input2 (H) Input2 (V)	—		Input pulse between 3 V and 5 V 
9 17 24 27 30	GND (V-SW) GND (H, V, Sync-Sep.) GND (B-out) GND (G-out) GND (R-out)	GND	—	—

Pin Description (M61323SP) (cont.)

pin No.	Name	DC Voltage (V)	Peripheral Circuit	Function
11	PwrSave-SW	2.5		Do not apply more 5 V DC voltage
13	CONT-SW	2.4		Do not apply more 5 V DC voltage
18 19	Vout Hout	—		—

Pin Description (M61323SP) (cont.)

pin No.	Name	DC Voltage (V)	Peripheral Circuit	Function
21	Sync sep OUT	—		—
22	Sync sep IN	—		Connect a capacitance between the pin and GND when not use SYNC-SEP
23	G Buffer OUT	—		—
25 28 31	Video OUT (B) Video OUT (G) Video OUT (R)	1.5		—

Note How to Use This IC (M61323SP)

1. R, G, B input signal is 0.7 V_{P-P} of standard video signal.
2. H, V input is 5.0 V TTL type.
3. Input signal with sufficient low impedance to input terminal.
4. The terminal of R, G, B output pin are shown as figure 1.
   When resistance is connected between the pin 31 (28, 25) and GND, I_{CC} will be increase.
5. Switch (pin 13) can be changed by supplying some voltage as figure 2.
   0 to 0.5 V: INPUT1
   2.5 to 5 V: INPUT2
   Do not apply V_{CC} or more DC voltage.
6. Power save mode is provided for saving I_{CC} less than about 10 mA as figure 3.
   0 to 0.5 V: Power save mode (H.V-SW, Sync-Sep., G-Buffer)
   2.5 to 5 V: Normal mode
   Do not apply 5 V or more DC voltage
7. When not use the Sync-separation circuit built in this IC, capacitance of several tens of pF is required between the pin 22 and GND.

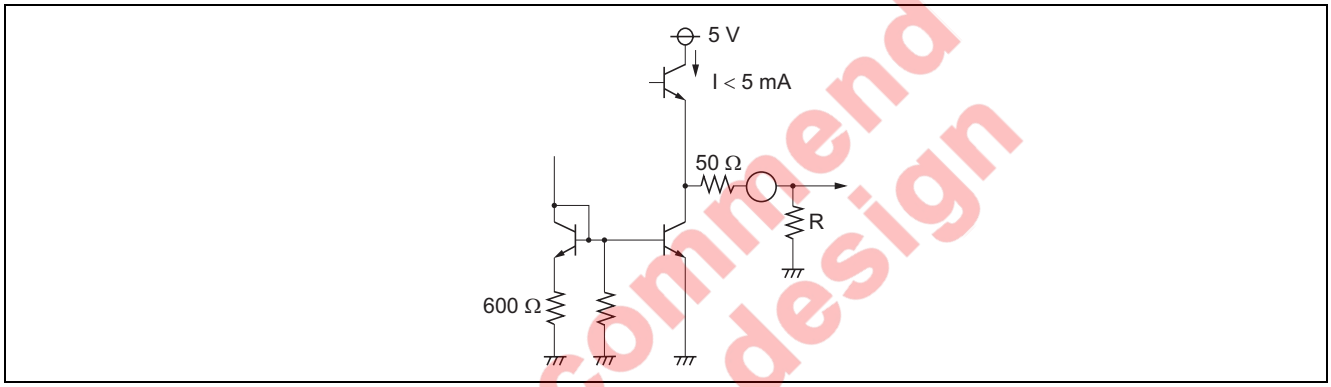


Figure 1

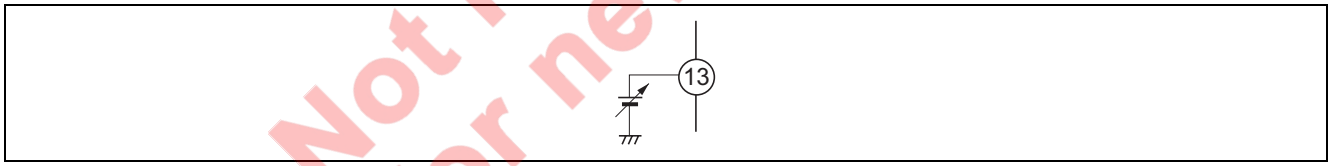


Figure 2

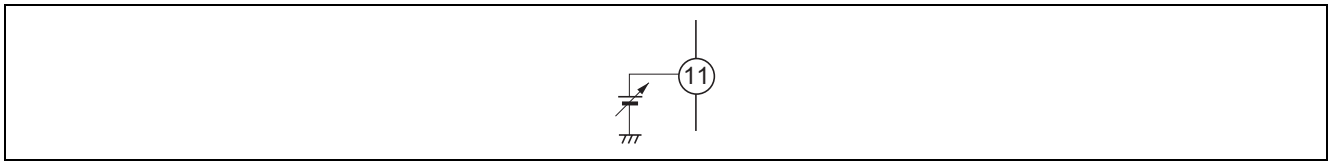


Figure 3

Cautions for Manufacturing Boards

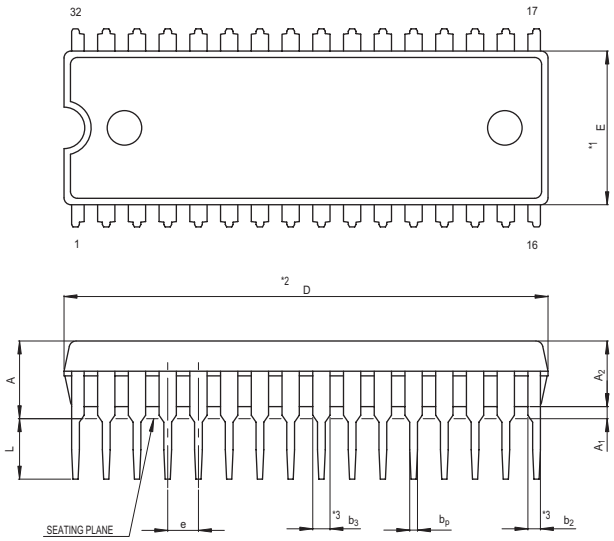
Built-in wide band preamplifier may cause oscillation due to the wiring shape on the board.

Be careful for the following points.

- V_{CC} shall use a stable power supply.
  (Individual V_{CC} should use an independent power supply.)
- GND should be as wide as possible. Basically, solid earth should be used.
  Make the load capacitance of output pins as small as possible.
- Also ground the hold capacitance to stable GND, which is as near to the pin as possible.
- Insertion of a resistance of several tens of ohms between the output pin and the circuit at the next stage makes oscillation harder.
- When inserting an output pull-down resistance, make wire between the output pin and the resistance as short as possible.

Package Dimensions

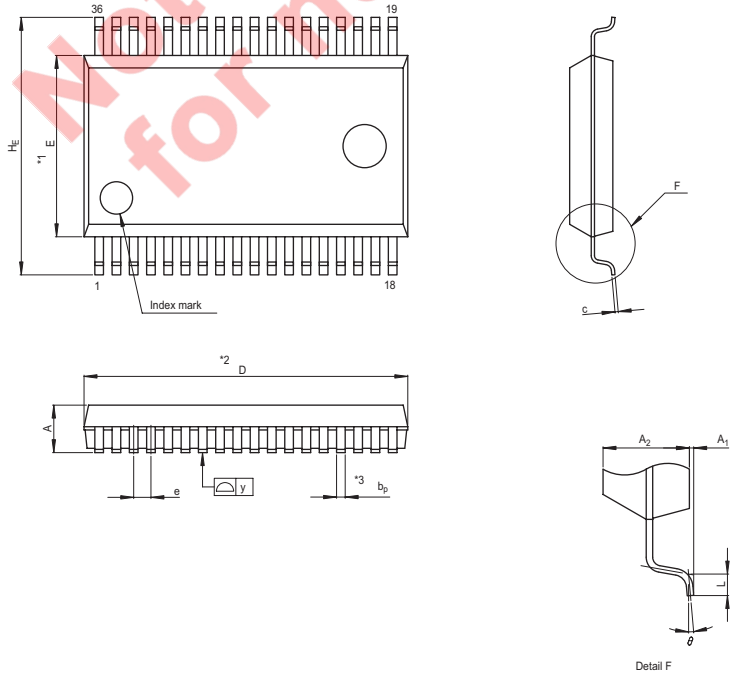
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SDIP32-8.9x28-1.78	PRDP0032BA-A	32P4B	2.2g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e1	9.86	10.16	10.46
D	27.8	28.0	28.2
E	8.75	8.9	9.05
A	—	—	5.08
A_1	0.51	—	—
A_2	—	3.8	—
b_p	0.35	0.45	0.55
b_2	0.63	0.73	1.03
b_3	0.9	1.0	1.3
c	0.22	0.27	0.34
θ	0°	—	15°
e	1.528	1.778	2.028
L	3.0	—	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SSOP36-8.4x15-0.80	PRSP0036GA-B	36P2R-D	0.5g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	14.8	15.0	15.2
E	8.2	8.4	8.6
A_2	—	2.05	—
A	—	—	2.35
A_1	0	0.1	0.2
b_p	0.3	0.35	0.45
c	0.18	0.2	0.25
θ	0°	—	8°
H_E	11.63	11.93	12.23
e	0.65	0.8	0.95
y	—	—	0.10
L	0.3	0.5	0.7

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Colophon .7.2